

## MEMORY

**CMOS 1 M × 4 BIT  
FAST PAGE MODE DRAM****MB814400A-60/-70/-80****CMOS 1,048,576 × 4 bit Fast Page Mode Dynamic RAM****DESCRIPTION**

The Fujitsu MB814400A is a fully decoded CMOS Dynamic RAM (DRAM) that contains a total of 4,194,304 memory cells accessible in 4-bit increments. The MB814400A features a "fast page" mode of operation whereby high-speed random access of up to 1,024-bits of data within the same row can be selected. The MB814400A DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB814400A is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB814400A is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814400A are not critical and all inputs are TTL compatible.

**PRODUCT LINE & FEATURES**

Parameter		MB814400A-60	MB814400A-70	MB814400A-80
RAS Access Time		60 ns max.	70 ns max.	80 ns max.
CAS Access Time		15 ns max.	20 ns max.	20 ns max.
Address Access Time		30 ns max.	35 ns max.	40 ns max.
Random Cycle Time		110 ns min.	125 ns min.	140 ns min.
Fast Page Mode Cycle Time		40 ns min.	45 ns min.	45 ns min.
Low power Dissipation	Operating current	605 mW max.	550 mW max.	495 mW max.
	Standby current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)		

- 1,048,576 words × 4 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 1024 refresh cycles every 16.4 ms
- Early write or  $\overline{OE}$  controlled write capability
- RAS only CAS-before-RAS, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

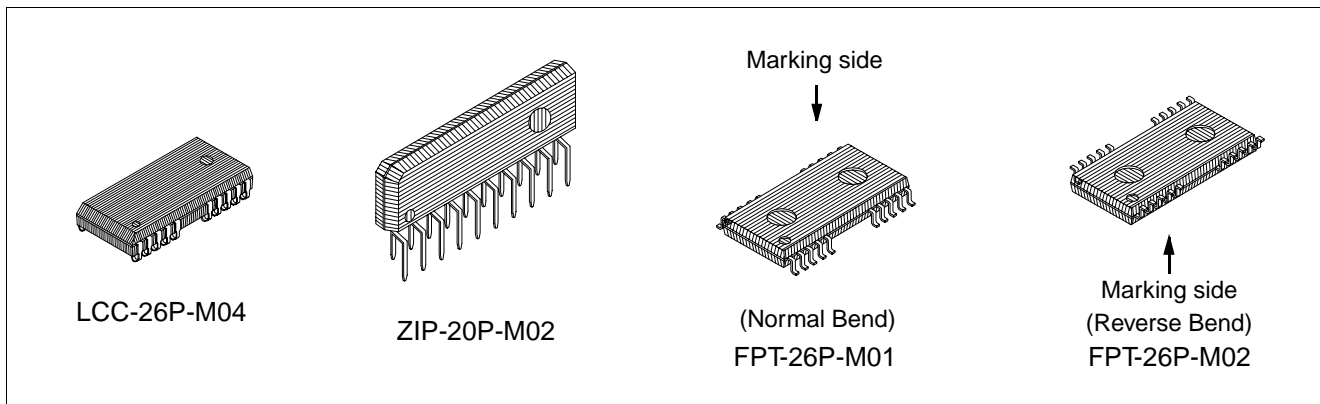
# MB814400A-60/MB814400A-70/MB814400A-80

## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-1 to +7	V
Voltage of $V_{CC}$ supply relative to $V_{SS}$	$V_{CC}$	-1 to +7	V
Power Dissipation	$P_D$	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	$T_{STG}$	-55 to +125	°C

**WARNING:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ■ PACKAGE

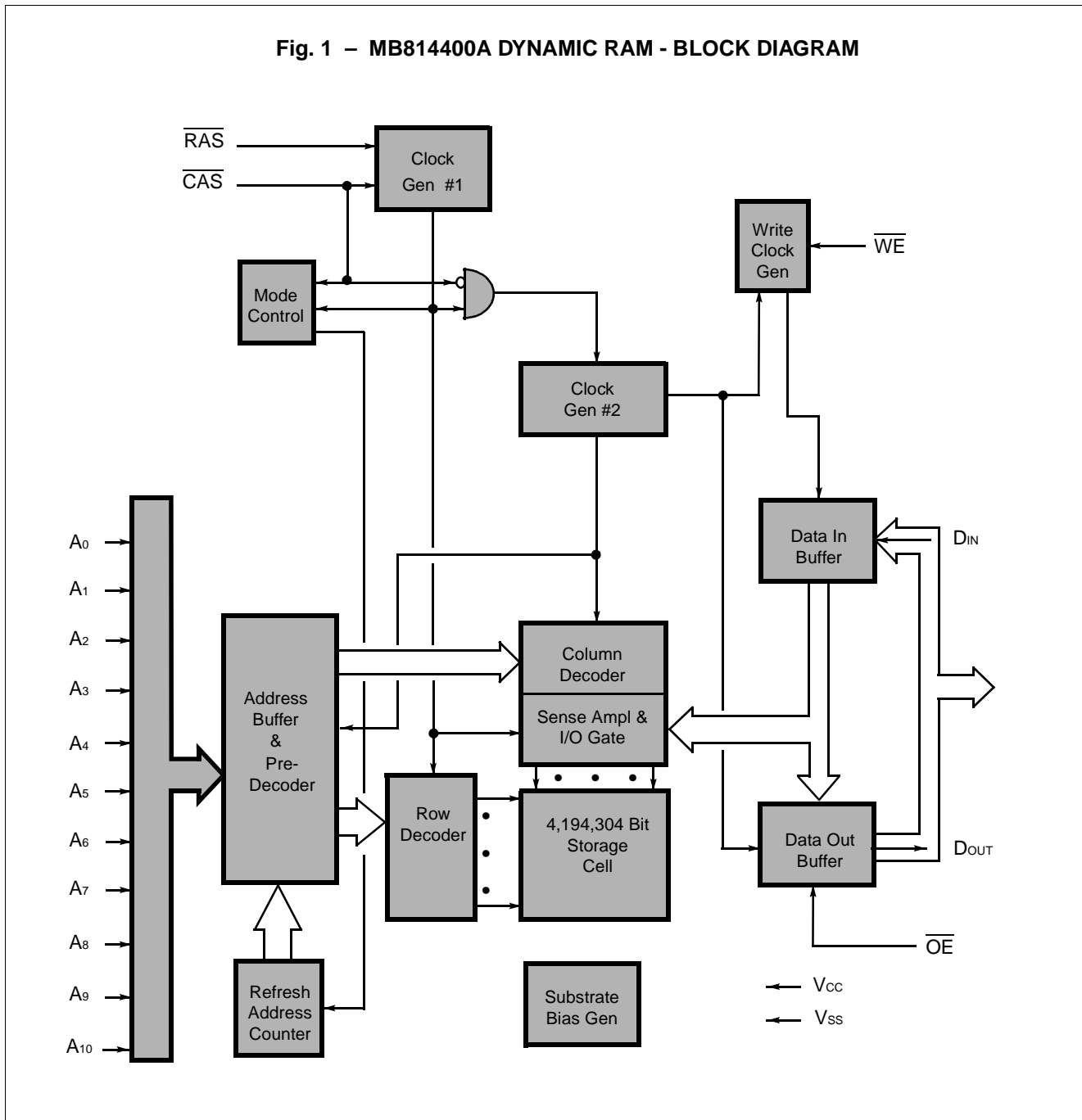


### Package and Ordering Information

- 26-pin plastic (300 mil) SOJ, order as MB814400A-xxPJN
- 20-pin plastic ZIP, order as MB814400A-xxPZ
- 26-pin plastic (300 mil) TSOP-II, with normal bend leads, order as MB814400A-xxPFTN
- 26-pin plastic (300 mil) TSOP-II, with reverse bend leads, order as MB814400A-xxPFTR

# MB814400A-60/MB814400A-70/MB814400A-80

Fig. 1 – MB814400A DYNAMIC RAM - BLOCK DIAGRAM



## ■ CAPACITANCE

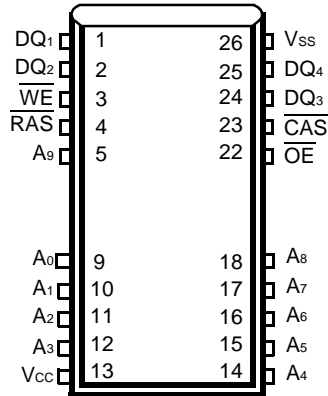
(T<sub>A</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A <sub>0</sub> to A <sub>9</sub> , D <sub>IN</sub>	C <sub>IN1</sub>	—	5	pF
Input Capacitance, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$	C <sub>IN2</sub>	—	7	pF
Input/Output Capacitance, DQ <sub>1</sub> to DQ <sub>4</sub>	C <sub>DQ</sub>	—	7	pF

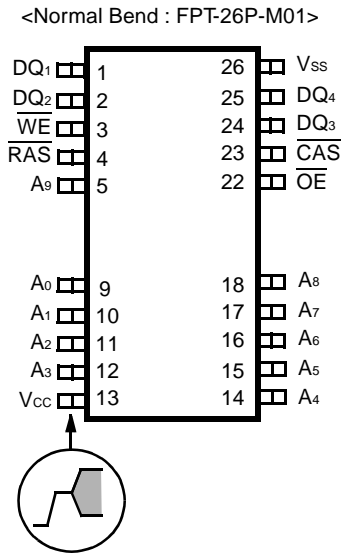
# MB814400A-60/MB814400A-70/MB814400A-80

## ■ PIN ASSIGNMENTS AND DESCRIPTIONS

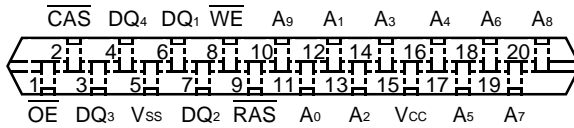
**26-Pin SOJ:**  
(Top View)



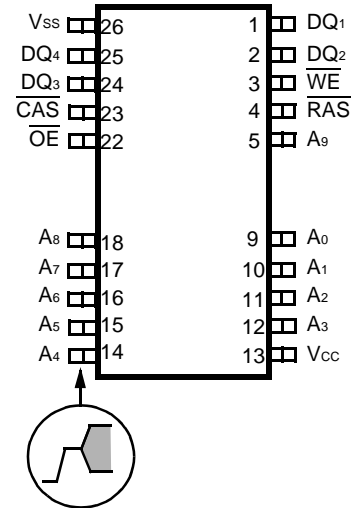
**26-Pin FPT:**  
(Top View)



**20-Pin ZIP:**  
(Top View)



<Reverse Bend : FPT-26P-M02>



Designator	Function
DQ <sub>1</sub> to DQ <sub>4</sub>	Data Input/Output
D <sub>OUT</sub>	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row Address Strobe.
A <sub>0</sub> to A <sub>9</sub>	No Connection.
V <sub>CC</sub>	Address Inputs.
$\overline{OE}$	+5 volt Power Supply.
$\overline{CAS}$	Column Address Strobe.
V <sub>SS</sub>	Circuit Ground.

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## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp.
Supply Voltage	1	$V_{CC}$	4.5	5.0	5.5	V	0°C to +70°C
		$V_{SS}$	0	0	0		
Input High Voltage, all inputs	1	$V_{IH}$	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	$V_{IL}$	-2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	$V_{ILD}$	-1.0	—	0.8	V	

\* : Undershoots of up to -2.0 volts with a pulse width not exceeding 20 ns are acceptable.

## ■ FUNCTIONAL OPERATION

### ADDRESS INPUTS

Twenty input bits are required to decode any four of 4,194,304 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by CAS and RAS as shown in Figure 5. First, ten row address bits are input on pins A<sub>0</sub>-through-A<sub>9</sub> and latched with the row address strobe (RAS) then, ten column address bits are input and latched with the column address strobe (CAS). Both row and column addresses must be stable on or before the falling edge of CAS and RAS, respectively. The address latches are of the flow-through type; thus, address information appearing after t<sub>RAH</sub> (min.)+ t<sub>T</sub> is automatically treated as the column address.

### WRITE ENABLE

The read or write mode is determined by the logic state of  $\overline{WE}$ . When  $\overline{WE}$  is active Low, a write cycle is initiated; when  $\overline{WE}$  is High, a read cycle is selected. During the read mode, input data is ignored.

### DATA INPUT

Input data is written into memory in either of three basic ways--an early write cycle, an  $\overline{OE}$  (delayed) write cycle, and a read-modify-write cycle. The falling edge of  $\overline{WE}$  or CAS, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data (DQ<sub>1</sub> to DQ<sub>4</sub>) is strobed by  $\overline{CAS}$  and the setup/hold times are referenced to CAS because  $\overline{WE}$  goes Low before CAS. In a delayed write or a read-modify-write cycle,  $\overline{WE}$  goes Low after CAS; thus, input data is strobed by  $\overline{WE}$  and all setup/hold times are referenced to the write-enable signal.

### DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- t<sub>RAC</sub> : from the falling edge of  $\overline{RAS}$  when t<sub>RCD</sub> (max.) is satisfied.
- t<sub>CAC</sub> : from the falling edge of CAS when t<sub>RCD</sub> is greater than t<sub>RCD</sub> (max.).
- t<sub>AA</sub> : from column address input when t<sub>RAD</sub> is greater than t<sub>RAD</sub> (max.).
- t<sub>OE</sub> : from the falling edge of  $\overline{OE}$  when  $\overline{OE}$  is brought Low after t<sub>RAC</sub>, t<sub>CAC</sub>, or t<sub>AA</sub>.

The data remains valid until either  $\overline{CAS}$  or  $\overline{OE}$  returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

### FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, RAS is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 1,024-bits can be accessed and, when multiple MB 814400s are used, CAS is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted.

# MB814400A-60/MB814400A-70/MB814400A-80

## ■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Note 3

Parameter	Notes	Symbol	Conditions	Values			Unit
				Min.	Typ.	Max.	
Output High Voltage	1	$V_{OH}$	$I_{OH} = -5 \text{ mA}$	2.4	—	—	V
Output Low Voltage	1	$V_{OL}$	$I_{OL} = 4.2 \text{ mA}$	—	—	0.4	
Input Leakage Current (Any Input)		$I_{I(L)}$	$0 \text{ V} \leq V_{IN} \leq 5.5 \text{ V};$ $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V};$ $V_{SS} = 0 \text{ V};$ All other pins not under test = $0 \text{ V}$	-10	—	10	$\mu\text{A}$
Output Leakage Current		$I_{DO(L)}$	$0 \text{ V} \leq V_{OUT} \leq 5.5 \text{ V};$ Data out disabled	-10	—	10	
Operating Current (Average Power Supply Current) 2	MB814400A-60	$I_{CC1}$	$\overline{\text{RAS}}$ & $\overline{\text{CAS}}$ cycling; $t_{RC} = \text{min.}$	—	—	110	mA
	MB814400A-70					100	
	MB814400A-80					90	
Standby Current (Power Supply Current)	TTL level	$I_{CC2}$	$\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$	—	—	2.0	mA
	CMOS level		$\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$			1.0	
Refresh Current#1 (Average Power Supply Current) 2	MB814400A-60	$I_{CC3}$	$\overline{\text{CAS}} = V_{IH}, \overline{\text{RAS}}$ cycling; $t_{RC} = \text{min.}$	—	—	110	mA
	MB814400A-70					100	
	MB814400A-80					90	
Fast Page Mode Current 2	MB814400A-60	$I_{CC4}$	$\overline{\text{RAS}} = V_{IL}, \overline{\text{CAS}}$ cycling; $t_{RC} = \text{min.}$	—	—	55	mA
	MB814400A-70					50	
	MB814400A-80					45	
Refresh Current#2 (Average Power Supply Current) 2	MB814400A-60	$I_{CC5}$	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}}$ -before-RAS; $t_{RC} = \text{min.}$	—	—	90	mA
	MB814400A-70					80	
	MB814400A-80					70	

# MB814400A-60/MB814400A-70/MB814400A-80

## ■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814400A-60		MB814400A-70		MB814400A-80		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
1	Time Between Refresh		$t_{REF}$	—	16.4	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		$t_{RC}$	110	—	125	—	140	—	ns
3	Read-Modify-Write Cycle Time		$t_{RWC}$	155	—	175	—	195	—	ns
4	Access Time from $\overline{RAS}$	6, 9	$t_{RAC}$	—	60	—	70	—	80	ns
5	Access Time from $\overline{CAS}$	7, 9	$t_{CAC}$	—	15	—	20	—	20	ns
6	Column Address Access Time	8, 9	$t_{AA}$	—	30	—	35	—	40	ns
7	Output Hold Time		$t_{OH}$	0	—	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		$t_{ON}$	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	$t_{OFF}$	—	15	—	15	—	20	ns
10	Transition Time		$t_T$	2	50	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		$t_{RP}$	40	—	45	—	50	—	ns
12	$\overline{RAS}$ Pulse Width		$t_{RAS}$	60	10000	70	10000	80	10000	ns
13	$\overline{RAS}$ Hold Time		$t_{RSH}$	15	—	20	—	20	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		$t_{CRP}$	5	—	5	—	5	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11, 12	$t_{RCD}$	20	45	20	50	20	60	ns
16	$\overline{CAS}$ Pulse Width		$t_{CAS}$	15	—	20	—	20	—	ns
17	$\overline{CAS}$ Hold Time		$t_{CSH}$	60	—	70	—	80	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	19	$t_{CPN}$	10	—	10	—	10	—	ns
19	Row Address Set Up Time		$t_{ASR}$	0	—	0	—	0	—	ns
20	Row Address Hold Time		$t_{RAH}$	10	—	10	—	10	—	ns
21	Column Address Set Up Time		$t_{ASC}$	0	—	0	—	0	—	ns
22	Column Address Hold Time		$t_{CAH}$	12	—	12	—	15	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	$t_{RAD}$	15	30	15	35	15	40	ns
24	Column Address to $\overline{RAS}$ Lead Time		$t_{RAL}$	30	—	35	—	40	—	ns
25	Column Address to $\overline{CAS}$ Lead Time		$t_{CAL}$	30	—	35	—	40	—	ns
26	Read Command Set Up Time		$t_{RCS}$	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{RAS}$	14	$t_{RRH}$	0	—	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{CAS}$	14	$t_{RCH}$	0	—	0	—	0	—	ns
29	Write Command Set Up Time	15	$t_{WCS}$	0	—	0	—	0	—	ns
30	Write Command Hold Time		$t_{WCH}$	10	—	10	—	12	—	ns

# MB814400A-60/MB814400A-70/MB814400A-80

## ■ AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

Notes 3, 4, 5

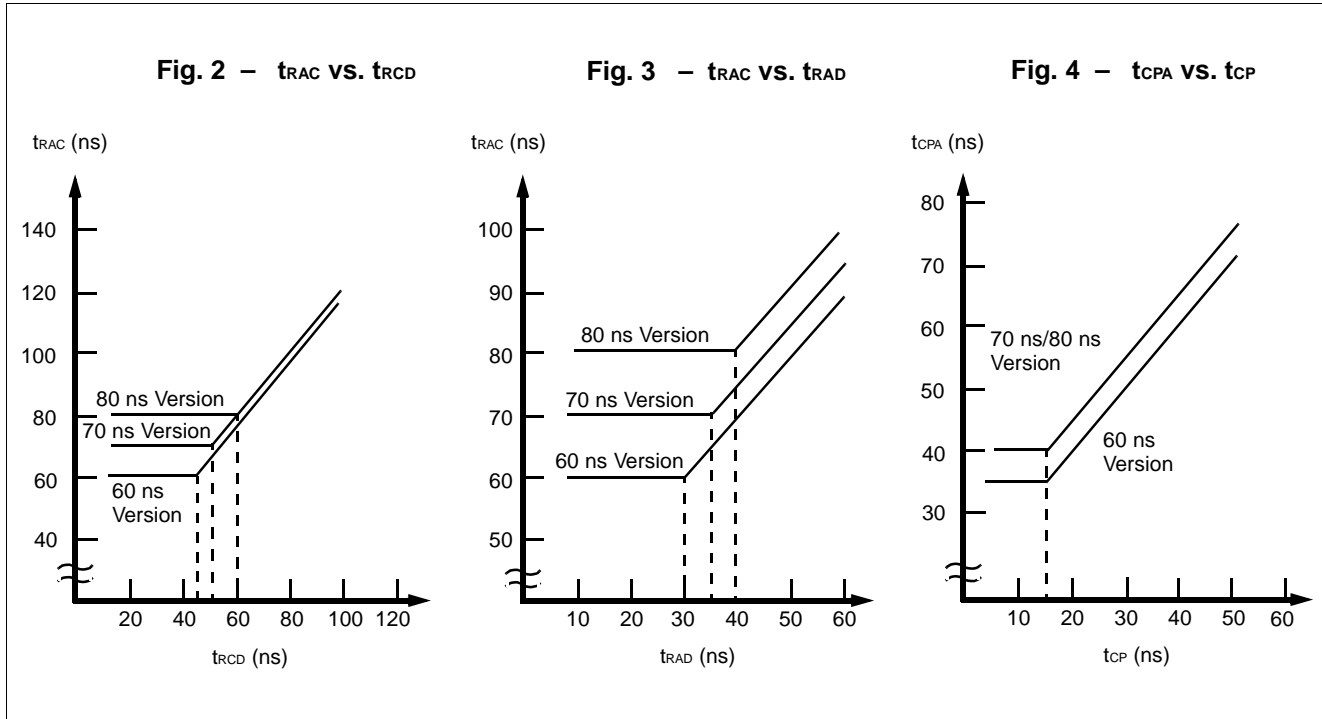
No.	Parameter	Notes	Symbol	MB814400A-60		MB814400A-70		MB814400A-80		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
31	WE Pulse Width		tWP	10	—	10	—	12	—	ns
32	Write Command to RAS Lead Time		tRWL	15	—	20	—	20	—	ns
33	Write Command to CAS Lead Time		tCWL	15	—	18	—	20	—	ns
34	D <sub>IN</sub> set Up Time		tDS	0	—	0	—	0	—	ns
35	D <sub>IN</sub> Hold Time		tDH	10	—	10	—	12	—	ns
36	RAS to WE Delay Time	15	tRWD	85	—	95	—	110	—	ns
37	CAS to WE Delay Time	15	tCWD	40	—	45	—	50	—	ns
38	Column Address to WE Delay Time	15	tAWD	55	—	60	—	70	—	ns
39	RAS Precharge Time to CAS Active Time (Refresh Cycles)		tRPC	0	—	0	—	0	—	ns
40	CAS Set Up Time for CAS-before-RAS Refresh		tCSR	0	—	0	—	0	—	ns
41	CAS Hold Time for CAS-before-RAS Refresh		tCHR	10	—	10	—	12	—	ns
42	WE SetUp Time from RAS	20	tWSR	0	—	0	—	0	—	ns
43	WE Hold Time from RAS	20	tWHR	10	—	10	—	10	—	ns
44	Access time from OE	9	tOEA	—	15	—	20	—	20	ns
45	Output Buffer Turn Off Delay from OE	10	tOEZ	—	15	—	15	—	20	ns
46	OE to RAS Lead Time for Valid Data		tOEL	10	—	10	—	10	—	ns
47	OE Hold Time Referenced to WE	16	tOEH	0	—	0	—	0	—	ns
48	OE to Data In Delay Time		tOED	15	—	15	—	20	—	ns
49	D <sub>IN</sub> to CAS Delay Time	17	tDZC	0	—	0	—	0	—	ns
50	D <sub>IN</sub> to OE Delay Time	17	tDZO	0	—	0	—	0	—	ns
51	Fast Page Mode Read/Write Cycle Time		tPC	40	—	45	—	45	—	ns
52	Fast Page Mode Read-Modify-Write Cycle Time		tPRWC	85	—	93	—	100	—	ns
53	Access Time from CAS Precharge	9, 18	tCPA	—	35	—	40	—	40	ns
54	Fast Page Mode CAS Precharge Time		tCP	10	—	10	—	10	—	ns
55	Fast Page Mode RAS Pulse width		tRASP	—	200000	—	200000	—	200000	ns
56	Fast Page Mode RAS Hold Time from CAS Precharge		tRHCP	35	—	40	—	40	—	ns
57	Fast Page Mode CAS Precharge to WE Delay Time		tCPWD	60	—	65	—	70	—	ns



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- Notes:
1. Referenced to  $V_{SS}$ .
  2.  $I_{CC}$  depends on the output load conditions and cycle rates; The specified values are obtained with the output open.  
 $I_{CC}$  depends on the number of address change as  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ ,  $V_{IL} > -0.5 V$ .  
 $I_{CC1}$ ,  $I_{CC3}$  and  $I_{CC5}$  are specified at one time of address change during  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .  
 $I_{CC4}$  is specified at one time of address change during one Page cycle.
  3. An Initial pause ( $\overline{RAS} = \overline{CAS} = V_{IH}$ ) of 200  $\mu s$  is required after power-up followed by any eight  $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight CAS-before-RAS initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
  4. AC characteristics assume  $t_T = 5$  ns.
  5.  $V_{IH}$  (min.) and  $V_{IL}$  (max.) are reference levels for measuring timing of input signals. Also transition times are measured between  $V_{IH}$  (min.) and  $V_{IL}$  (max.).
  6. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max.})$ ,  $t_{RAD} \leq t_{RAD}(\text{max.})$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will be increased by the amount that  $t_{RCD}$  exceeds the value shown. Refer to Fig. 2 and 3.
  7. If  $t_{RCD} \geq t_{RCD}(\text{max.})$ ,  $t_{RAD} \geq t_{RAD}(\text{max.})$ , and  $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{CAC}$ .
  8. If  $t_{RAD} \geq t_{RAD}(\text{max.})$  and  $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{AA}$ .
  9. Measured with a load equivalent to two TTL loads and 100 pF.
  10.  $t_{OFF}$  and  $t_{OEZ}$  is specified that output buffer change to high impedance state.
  11. Operation within the  $t_{RCD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  12.  $t_{RCD}(\text{min.}) = t_{RAH}(\text{min.}) + 2t_T + t_{ASC}(\text{min.})$ .
  13. Operation within the  $t_{RAD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  14. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
  15.  $t_{WCS}$  is specified as a reference point only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$  the data output pin will remain High-Z state through entire cycle.
  16. Assumes that  $t_{WCS} < t_{WCS}(\text{min.})$
  17. Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
  18.  $t_{CPA}$  is access time from the selection of a new column address (that is caused by changing  $\overline{CAS}$  from "L" to "H"). Therefore, if  $t_{CP}$  is long,  $t_{CPA}$  is longer than  $t_{CPA}(\text{max.})$ .
  19. Assumes that CAS-before-RAS refresh.
  20. Assumes that Test mode function.

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## FUNCTIONAL TRUTH TABLE

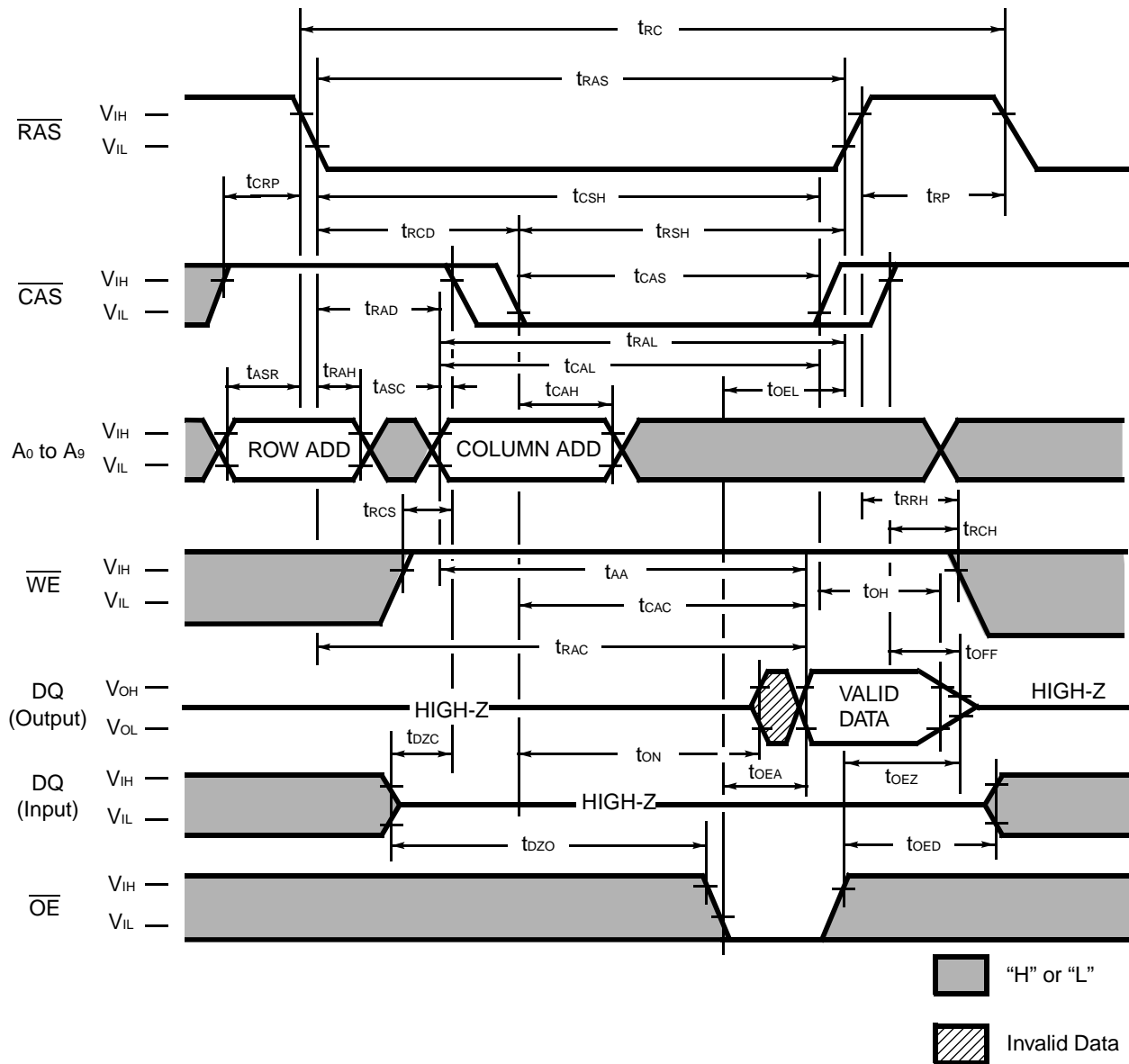
Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes*	$t_{RCS} \geq t_{RCS} (\text{min.})$
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	Yes*	$t_{WCS} \geq t_{WCS} (\text{min.})$
Read-Modify-Write Cycle	L	L	H $\rightarrow$ L	L $\rightarrow$ H	Valid	Valid	Valid	Valid	Yes*	$t_{CWD} \geq t_{CWD} (\text{min.})$
$\overline{RAS}$ -only Refresh Cycle	L	H	X	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$ -before- $\overline{RAS}$ Refresh Cycle	L	L	H	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR} (\text{min.})$
Hidden Refresh Cycle	H $\rightarrow$ L	L	H	L	—	—	—	Valid	Yes	Previous data is kept.
Test mode set Cycle (CBR)	L	L	L	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR} (\text{min.})$ $t_{WSR} \geq t_{WSR} (\text{min.})$
Test Mode Set Cycle (Hidden)	H $\rightarrow$ L	L	L	X	—	—	—	Valid	Yes	$t_{CSR} \geq t_{CSR} (\text{min.})$ $t_{WSR} \geq t_{WSR} (\text{min.})$

Note: X : "H" or "L"

\*1: It is impossible in Fast Page Mode.

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Fig. 5 - READ CYCLE



## DESCRIPTION

To implement a read operation, a valid address is latched in by the  $\overline{RAS}$  and  $\overline{CAS}$  address strobes and with  $\overline{WE}$  set to a High level and  $\overline{OE}$  set to a low level, the output is valid once the memory access time has elapsed. The access time is determined by  $\overline{RAS}$  ( $t_{RAC}$ ),  $\overline{CAS}$  ( $t_{CAC}$ ),  $\overline{OE}$  ( $t_{OEA}$ ) or column addresses ( $t_{AA}$ ) under the following conditions:

If  $t_{RCD} > t_{RCD}(\max.)$ , access time =  $t_{CAC}$ .

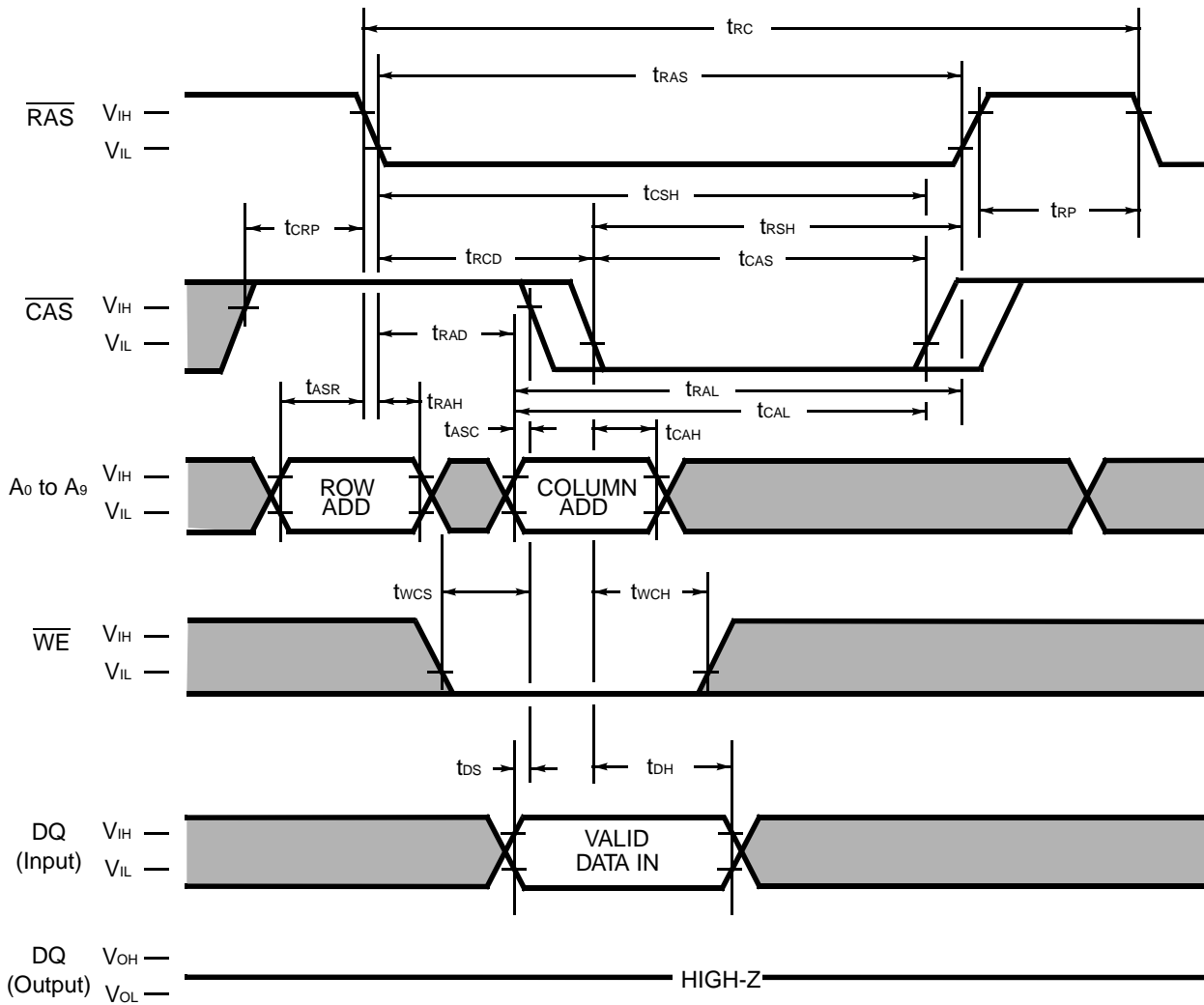
If  $t_{RAD} > t_{RAD}(\max.)$ , access time =  $t_{AA}$ .

If  $\overline{OE}$  is brought Low after  $t_{RAC}$ ,  $t_{CAC}$ , or  $t_{AA}$  (which ever occurs later), access time =  $t_{OEA}$ .

However, if either  $\overline{CAS}$  or  $\overline{OE}$  goes High, the output returns to a high-impedance state after  $t_{OH}$  is satisfied.

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Fig. 6 - EARLY WRITE CYCLE ( $\overline{OE}$  = "H" or "L")

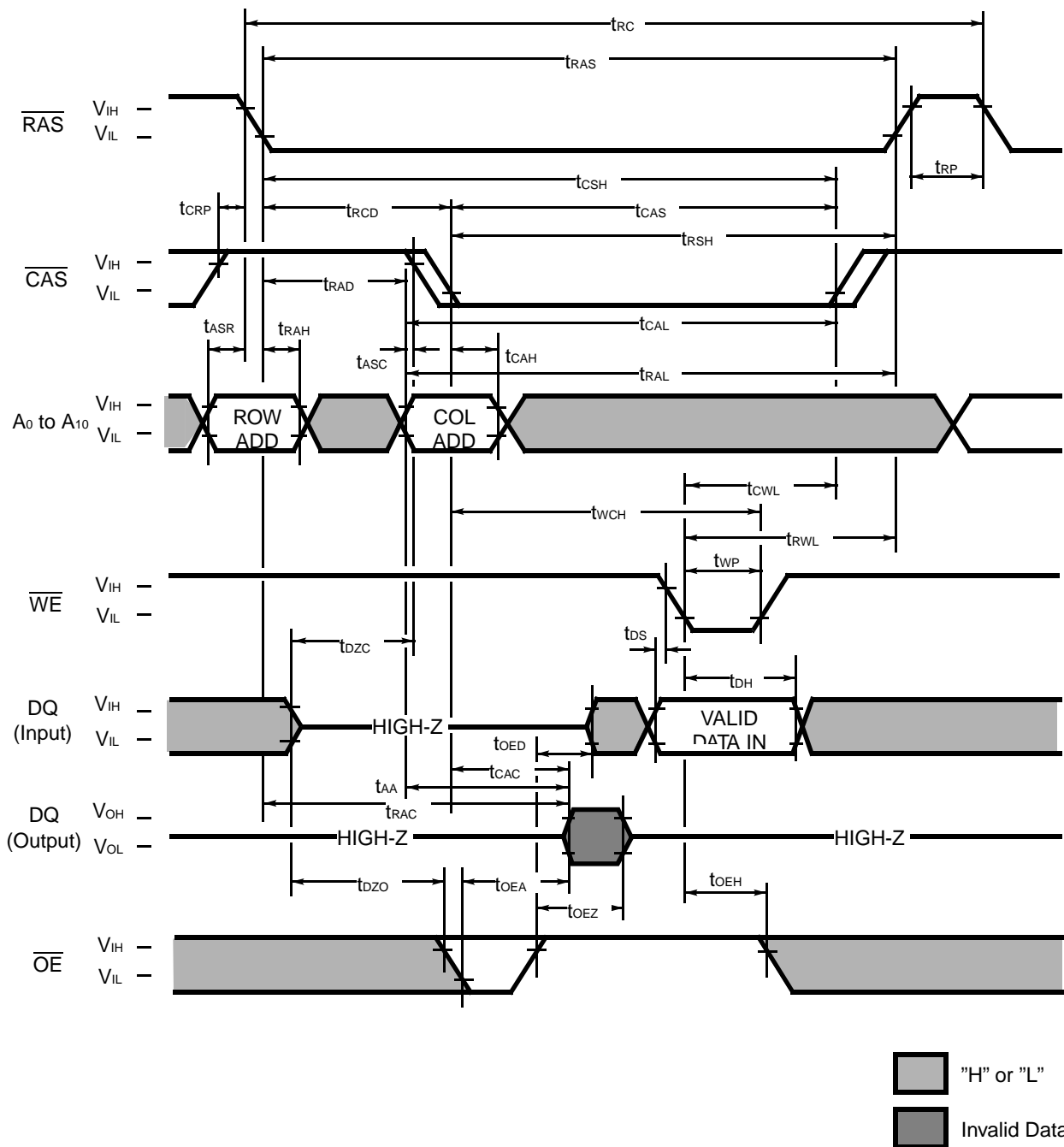


 "H" or "L"

**DESCRIPTION**

A write cycle is similar to a read cycle except  $\overline{WE}$  is set to a Low state and  $\overline{OE}$  is a "H" or "L" signal. A write cycle can be implemented in either or three ways - early write,  $\overline{OE}$  write (delayed write), or read-modify-write. During all write cycles, timing parameters  $t_{RWL}$ ,  $t_{CWL}$  and  $t_{RAL}$  must be satisfied. In the early write cycle shown above  $t_{WCS}$  satisfied, data on the DQ pin is latched with the falling edge of  $\overline{CAS}$  and written into memory.

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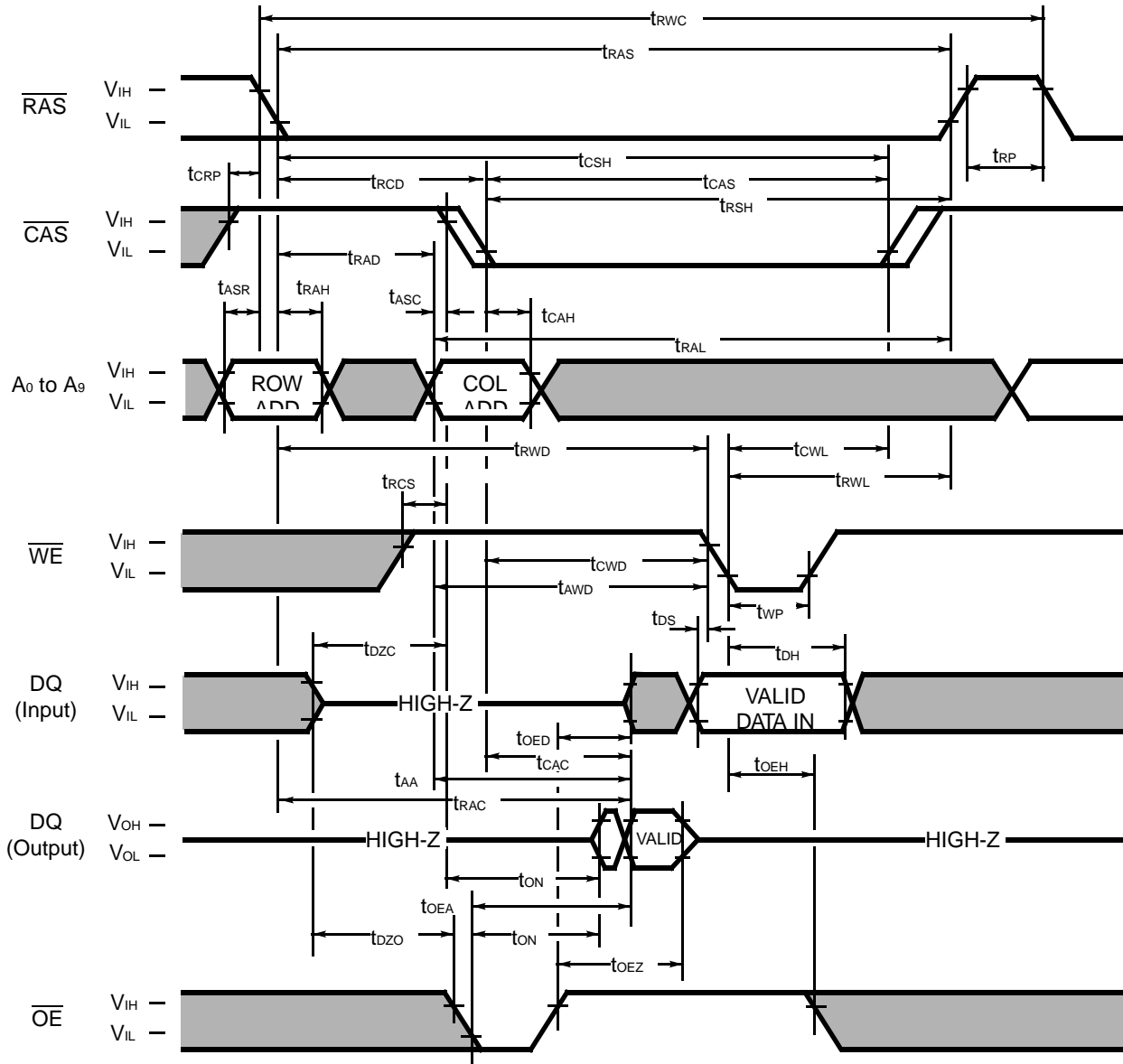
Fig. 7 -  $\overline{\text{OE}}$  (DELAYED WRITE CYCLE)


## DESCRIPTION

In the  $\overline{\text{OE}}$  (delayed write) cycle,  $t_{WCS}$  is not satisfied; thus, the data on the DQ pins is latched with the falling edge of  $\overline{\text{WE}}$  and written into memory. The Output Enable ( $\overline{\text{OE}}$ ) signal must be changed from Low to High before  $\overline{\text{WE}}$  goes Low ( $t_{OED} + t_r + t_{DS}$ ).

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Fig. 8 - READ-MODIFY-WRITE-CYCLE



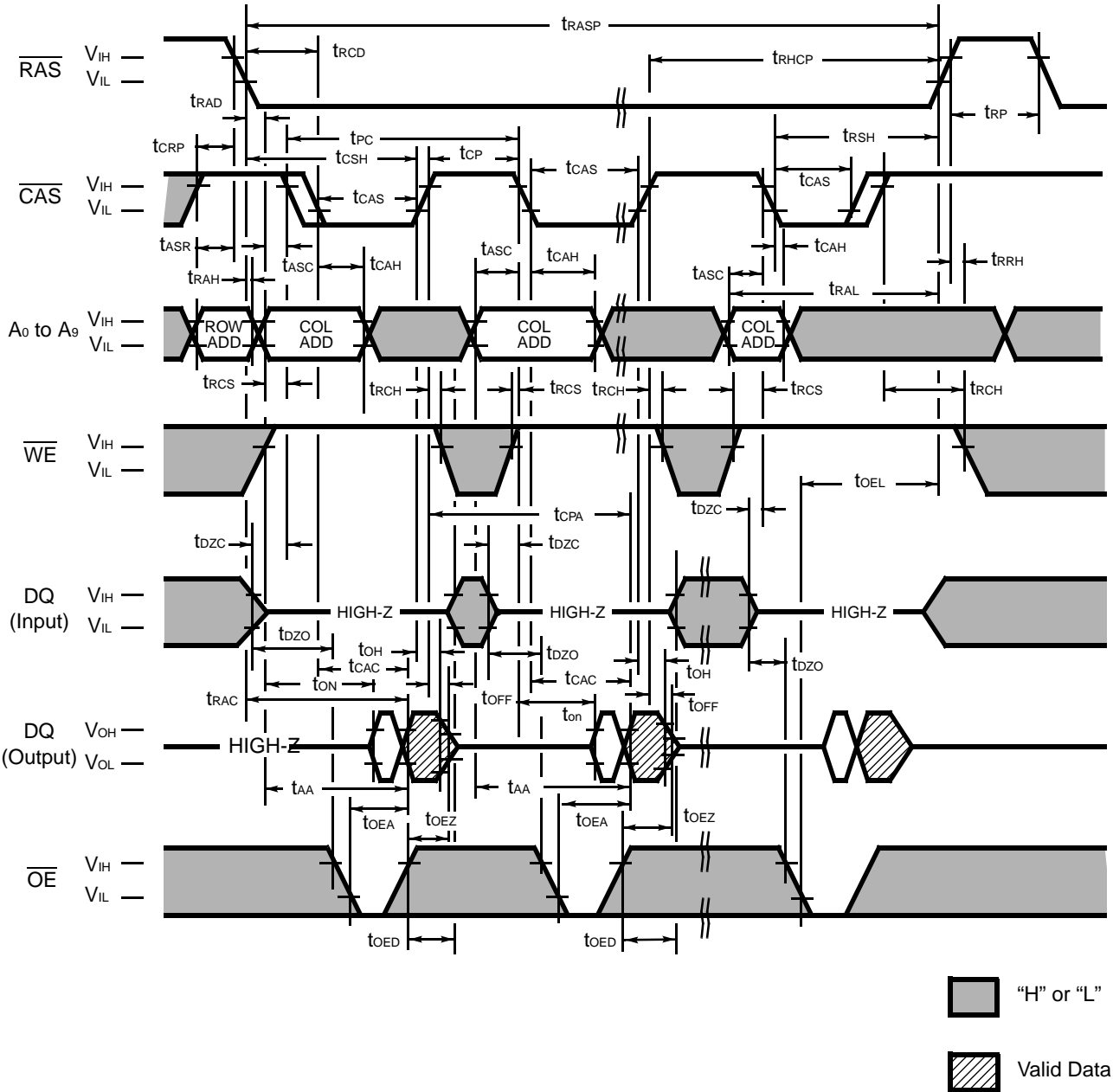
 "H" or "L"

DESCRIPTION

The read-modify-write cycle is executed by changing  $\overline{WE}$  from High to Low after the data appears on the DQ pins. In the read-modify-write cycle,  $\overline{OE}$  must be changed from Low to High after the memory access time.

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Fig. 9 - FAST PAGE MODE READ CYCLE (Early Write)

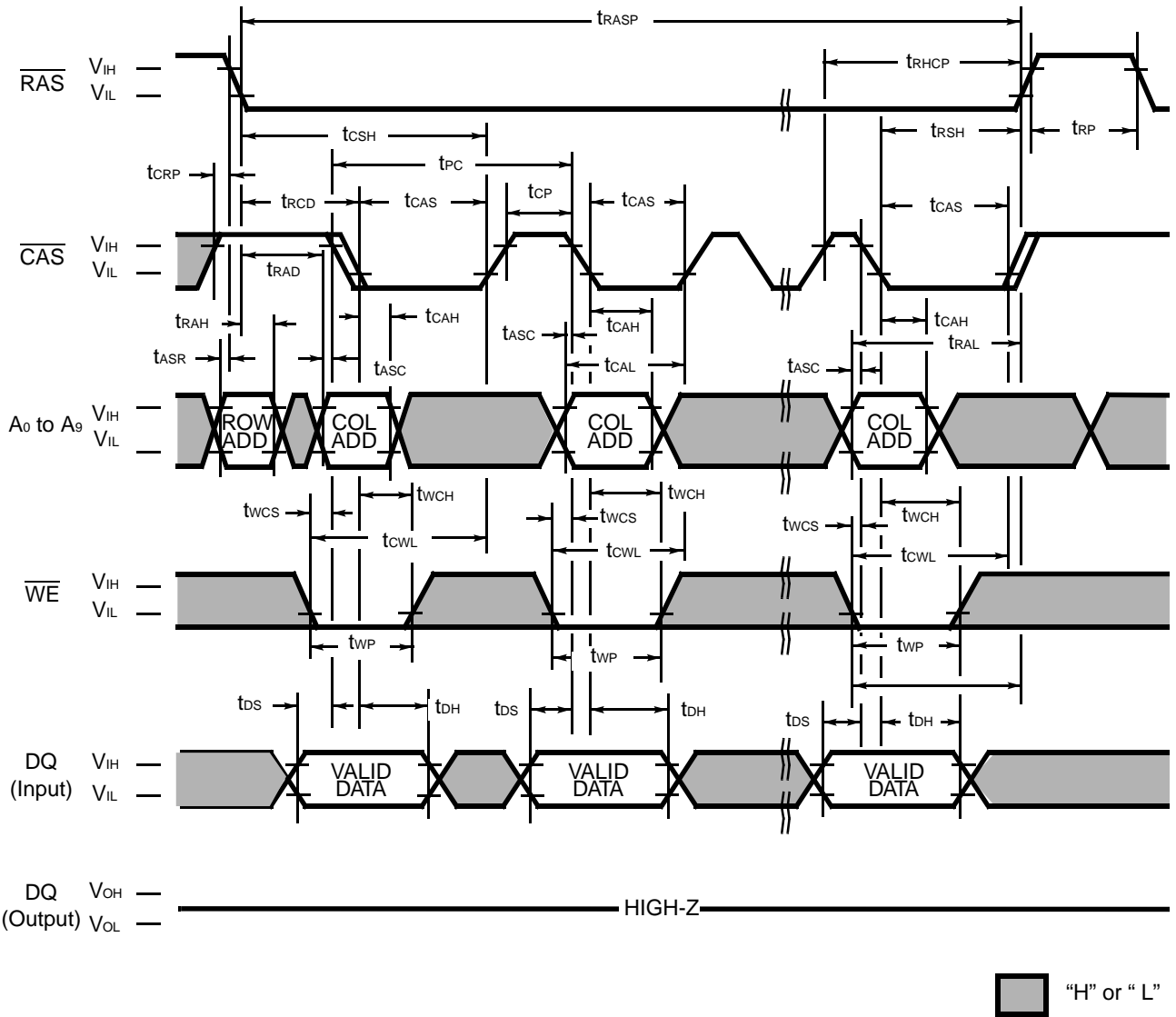


DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining RAS at a Low level and WE at a High level during all successive memory cycles in which the row address is latched. The access time is determined by  $t_{CAC}$ ,  $t_{AA}$ ,  $t_{CPA}$ , or  $t_{OEA}$ , whichever one is the latest in occurring.

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Fig. 10 - FAST PAGE MODE WRITE CYCLE ( $\overline{OE}$  = "H" or "L")



DESCRIPTION

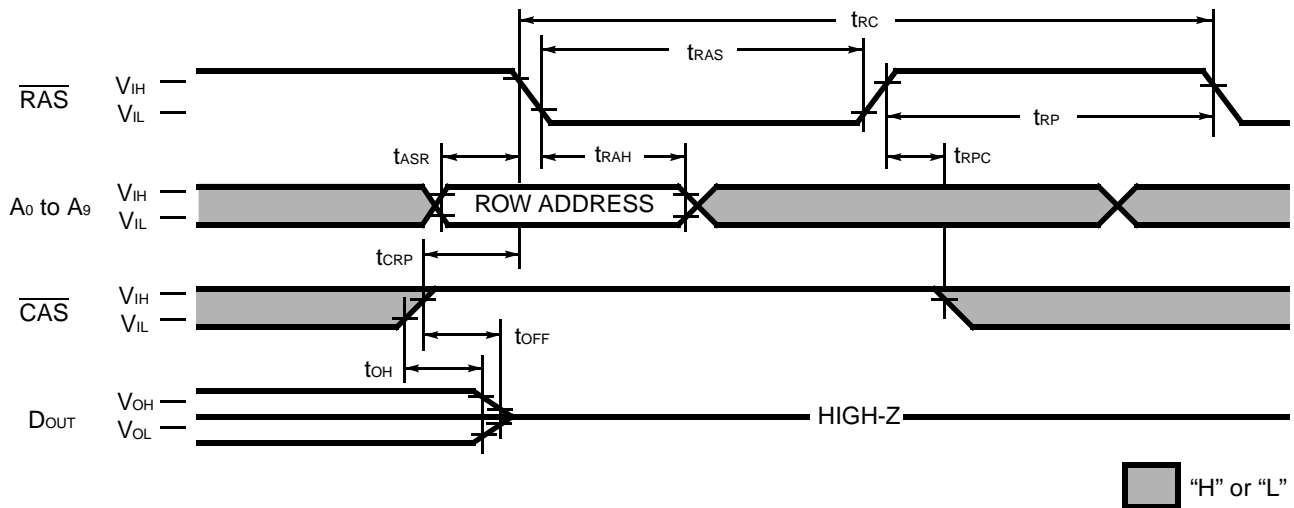
The fast page mode write cycle is executed in the same manner as the fast page mode read cycle except for the states of  $\overline{WE}$  and  $\overline{OE}$  are reversed. Data appearing on the DQ pins is latched on the falling edge of CAS and written into memory. During the fast page mode write cycle, including the delayed ( $\overline{OE}$ ) write and read-modify-write cycles,  $t_{CWL}$  must be satisfied.





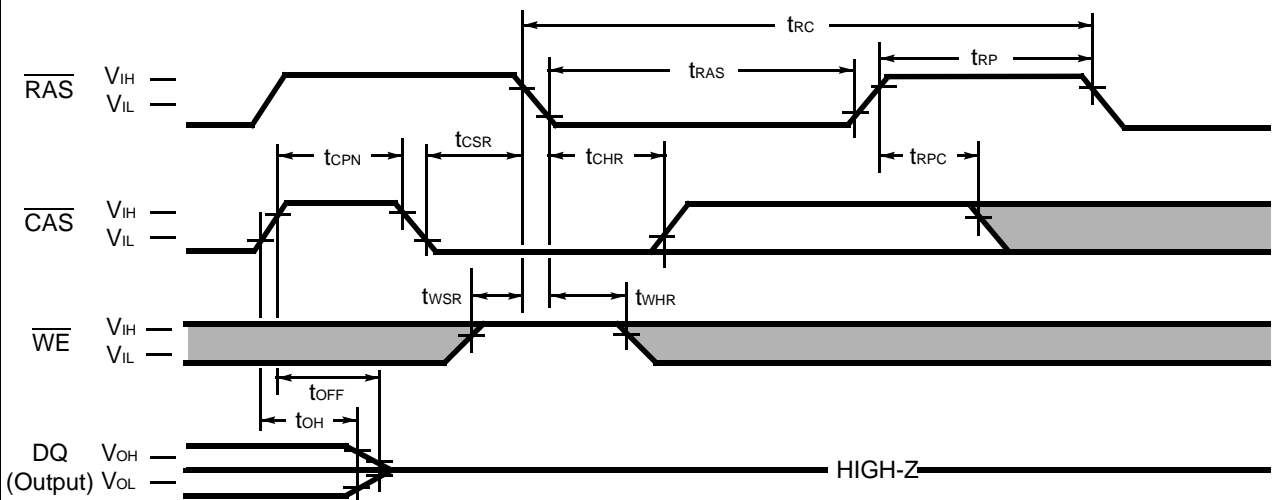


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Fig. 13 -  $\overline{\text{RAS}}$ -ONLY REFRESH ( $\overline{\text{WE}} = \overline{\text{OE}} = \text{"H"}$  or  $\text{"L"}$ )

## DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 1024 row addresses every 16.4-milliseconds. Three refresh modes are available:  $\overline{\text{RAS}}$ -only refresh,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh, and hidden refresh.  $\overline{\text{RAS}}$ -only refresh is performed by keeping  $\overline{\text{RAS}}$  Low and  $\overline{\text{CAS}}$  High throughout the cycle; the row address to be refreshed is latched on the falling edge of  $\overline{\text{RAS}}$ . During  $\overline{\text{RAS}}$ -only refresh, DQ pin is kept in a high-impedance state.

Fig. 14 -  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH (ADDRESSES =  $\overline{\text{OE}} = \text{"H"}$  or  $\text{"L"}$ )

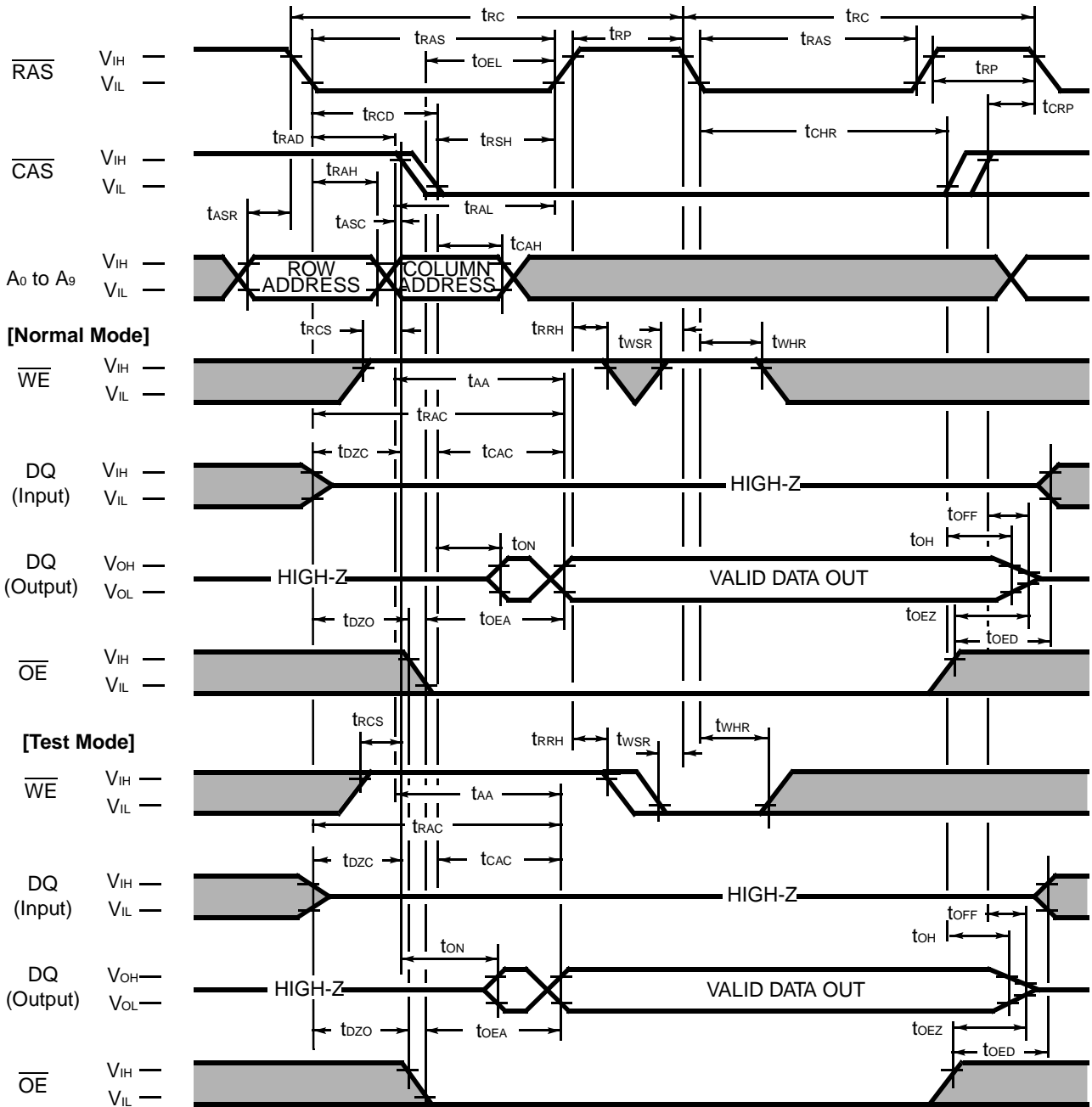
## DESCRIPTION

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If  $\overline{\text{CAS}}$  is held Low for the specified setup time ( $t_{\text{CSR}}$ ) before  $\overline{\text{RAS}}$  goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh operation.

$\overline{\text{WE}}$  must be held High for the specified set up time ( $t_{\text{WSR}}$ ) before  $\overline{\text{RAS}}$  goes low in order not to enter "test mode".

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Fig. 15 – HIDDEN REFRESH CYCLE



■ "H" or "L"

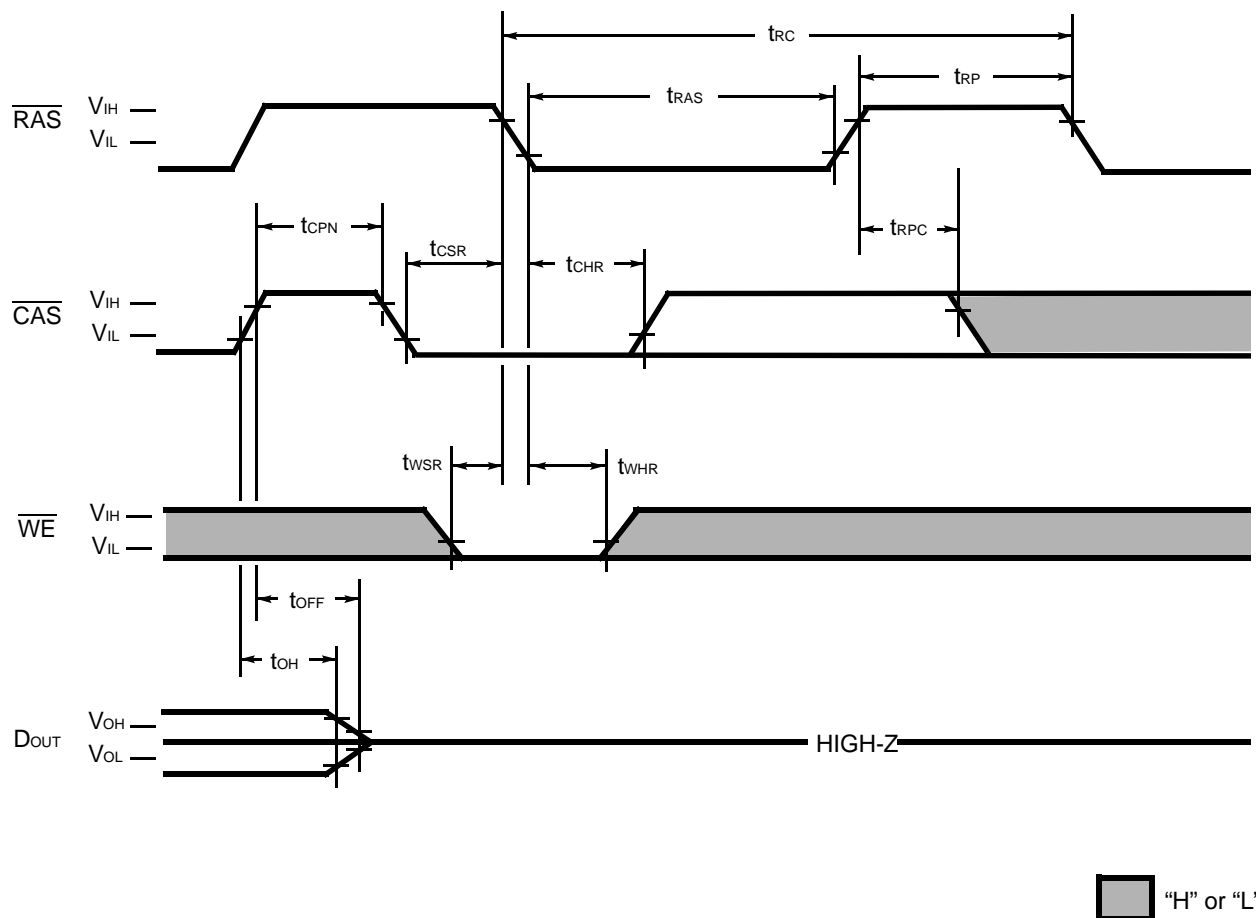
DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of  $\overline{\text{CAS}}$  and cycling  $\overline{\text{RAS}}$ . The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability.

$\overline{\text{WE}}$  must be held High for the specified set up time ( $t_{\text{WSR}}$ ) before  $\overline{\text{RAS}}$  goes Low in order not to enter "test mode".

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Fig. 16 – TEST MODE SET CYCLE ( $A_0$  to  $A_9$ ,  $\overline{OE} = \text{"H" or "L"}$ )



## DESCRIPTION

Test Mode ;

The purpose of this test mode is to reduce device test time to one eighth of that required to test the device conventionally. The test mode function is entered by performing a  $\overline{WE}$  and  $\overline{CAS}$ -before- $\overline{RAS}$  (WCBR) refresh for the entry cycle.

In the test mode, read and write operations are executed in units of eight bits which are selected by the address combination of  $RA_{10}$ ,  $CA_0$  and  $CA_{10}$ . In the write mode, data at  $D_{IN}$  is written into eight cells simultaneously. But the data must be input from  $DQ_2$  only. In the read mode, the data of eight cells at the selected addresses are read back out from  $DQ$  and checked in the following manner.

When the eight bits are all "L" or all "H", a "H" level is output.

When the eight bits show a combination of "L" and "H", a "L" level is output.

The test mode function is exited by performing a  $\overline{RAS}$ -only refresh or a  $\overline{CAS}$ -before- $\overline{RAS}$  refresh for the exit cycle.

In test mode operation, the following parameters are delayed approximately 5 ns from the specified value in the data sheet.

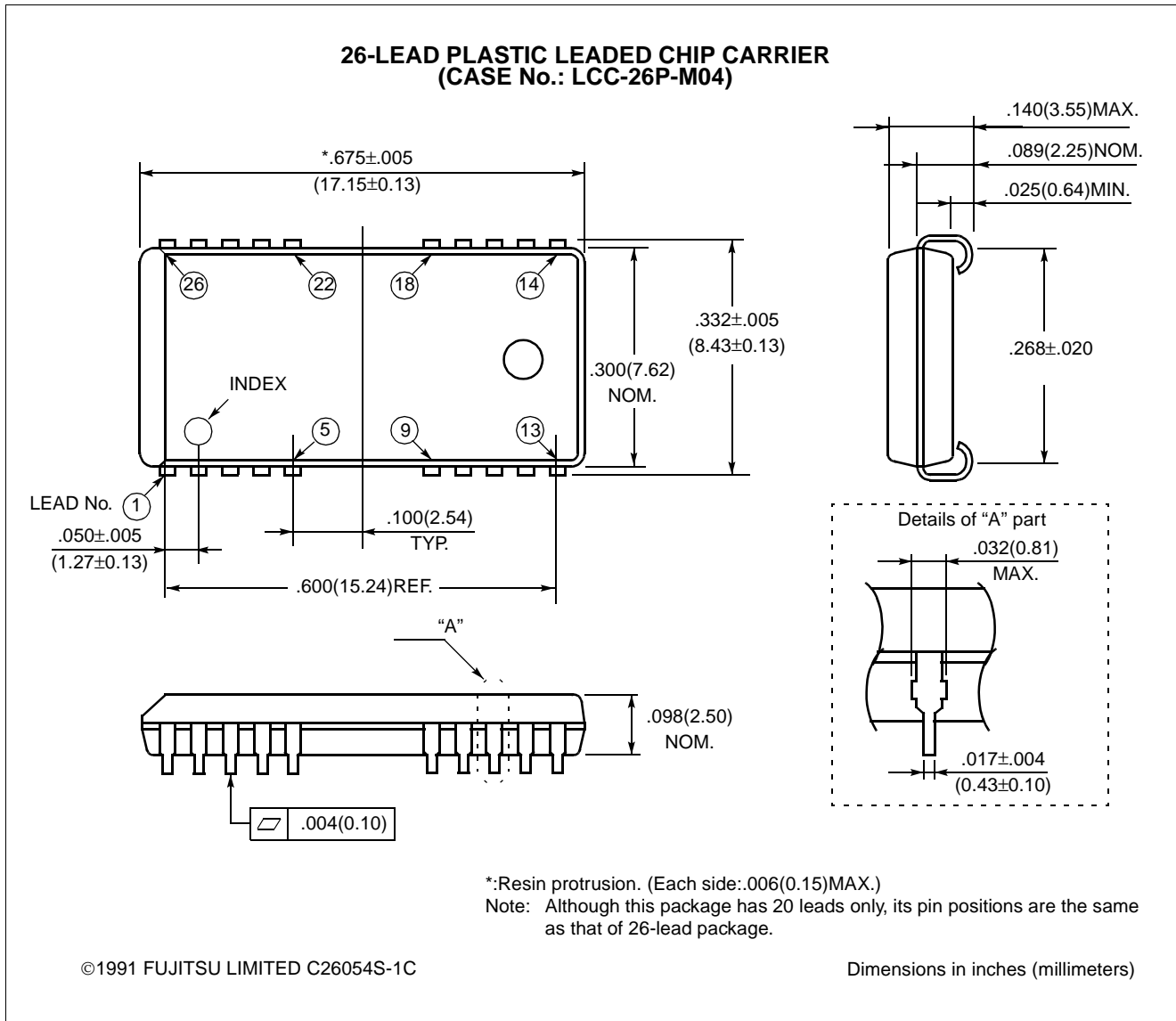
$t_{RC}$ ,  $t_{RWC}$ ,  $t_{TRAC}$ ,  $t_{AA}$ ,  $t_{RAS}$ ,  $t_{CSH}$ ,  $t_{RAL}$ ,  $t_{RWD}$ ,  $t_{AWD}$ ,  $t_{PC}$ ,  $t_{PRWC}$ ,  $t_{CPA}$ ,  $t_{RHCP}$ ,  $t_{CPWD}$



# MB814400A-60/MB814400A-70/MB814400A-80

## ■ PACKAGE DIMENSIONS

(Suffix: -PJN)



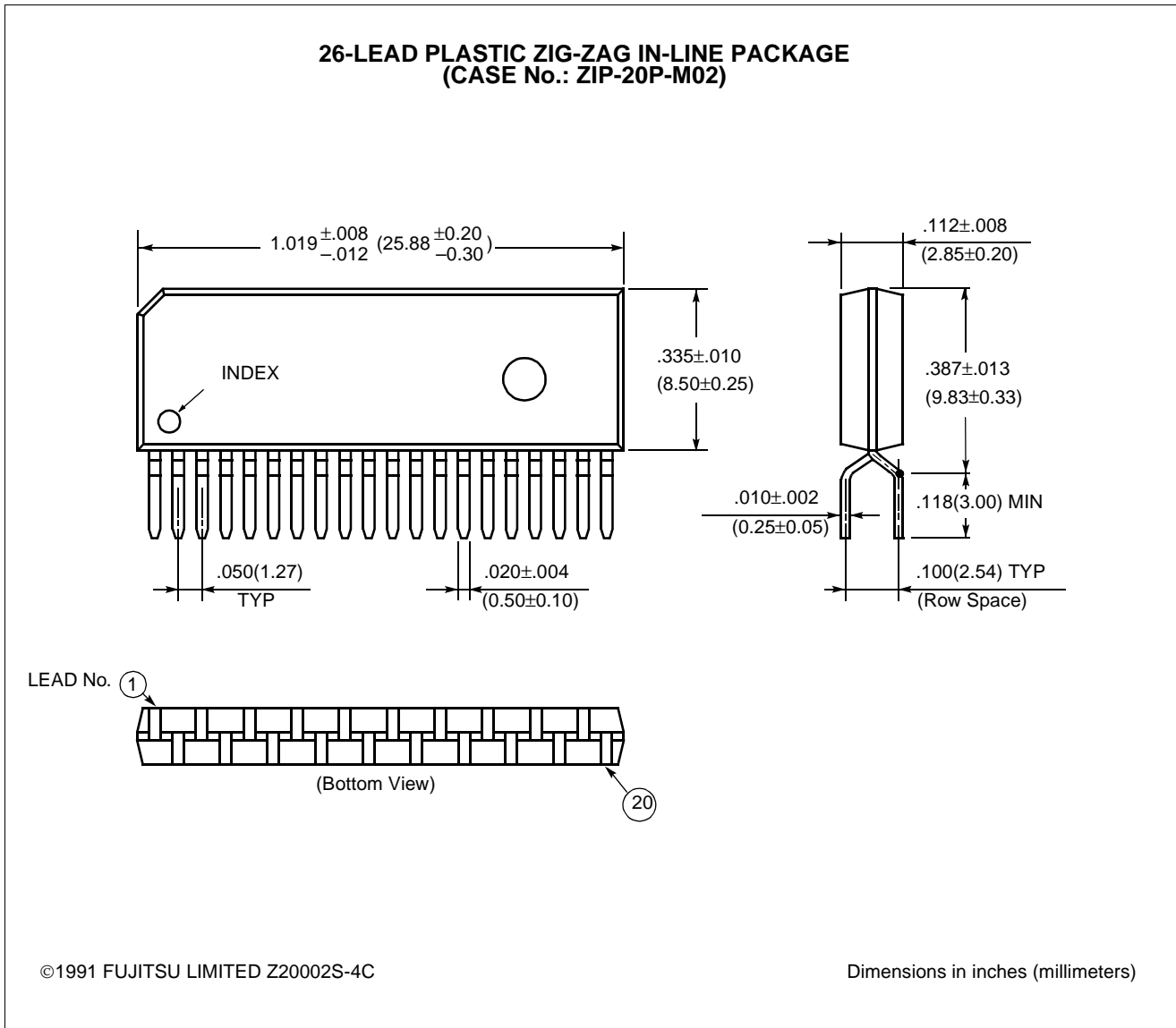
\*:Resin protrusion. (Each side:.006(0.15)MAX.)

Note: Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

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## ■ PACKAGE DIMENSIONS (Continued)

(Suffix: -PZ)

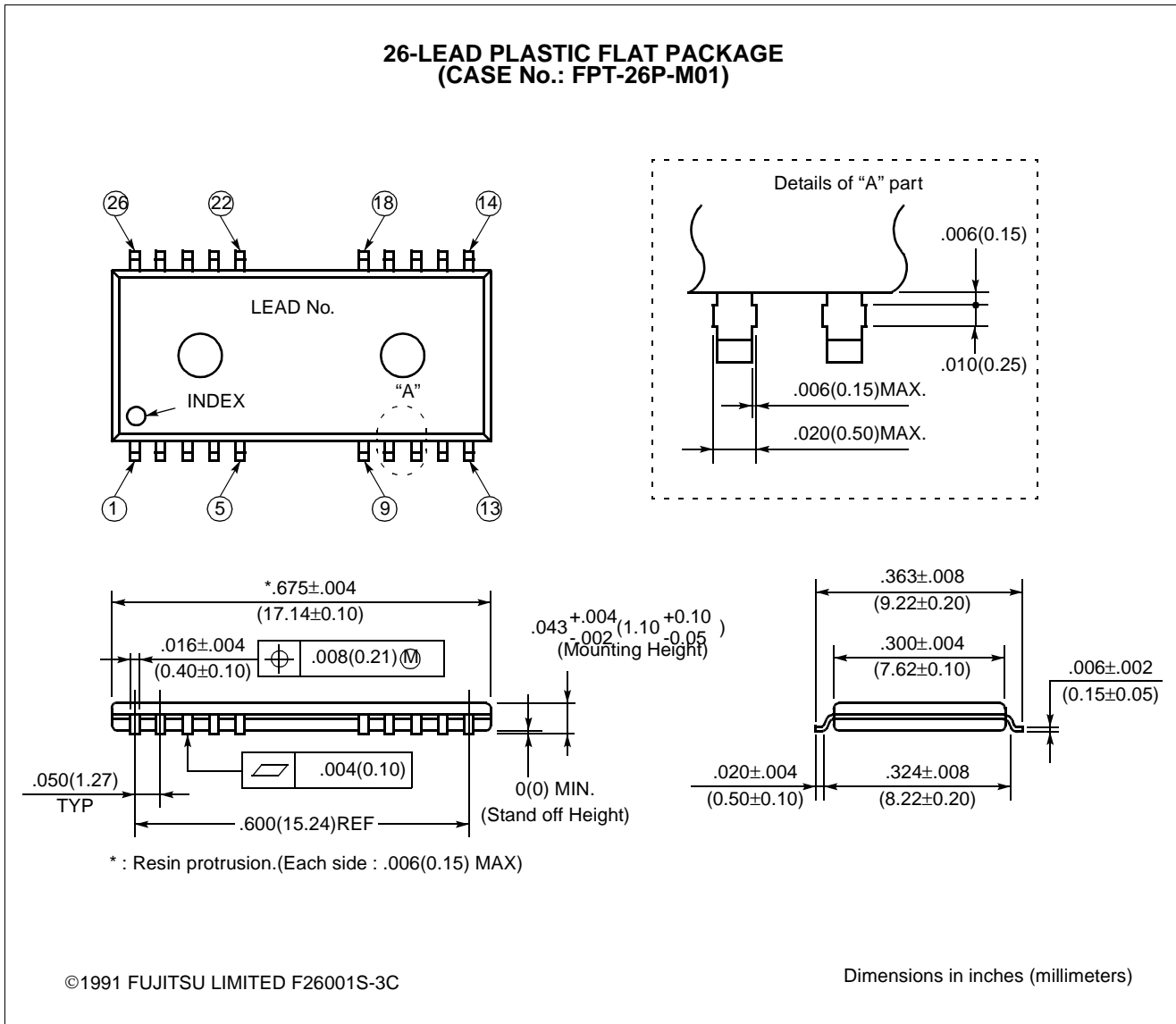




# MB814400A-60/MB814400A-70/MB814400A-80

## ■ PACKAGE DIMENSIONS (Continued)

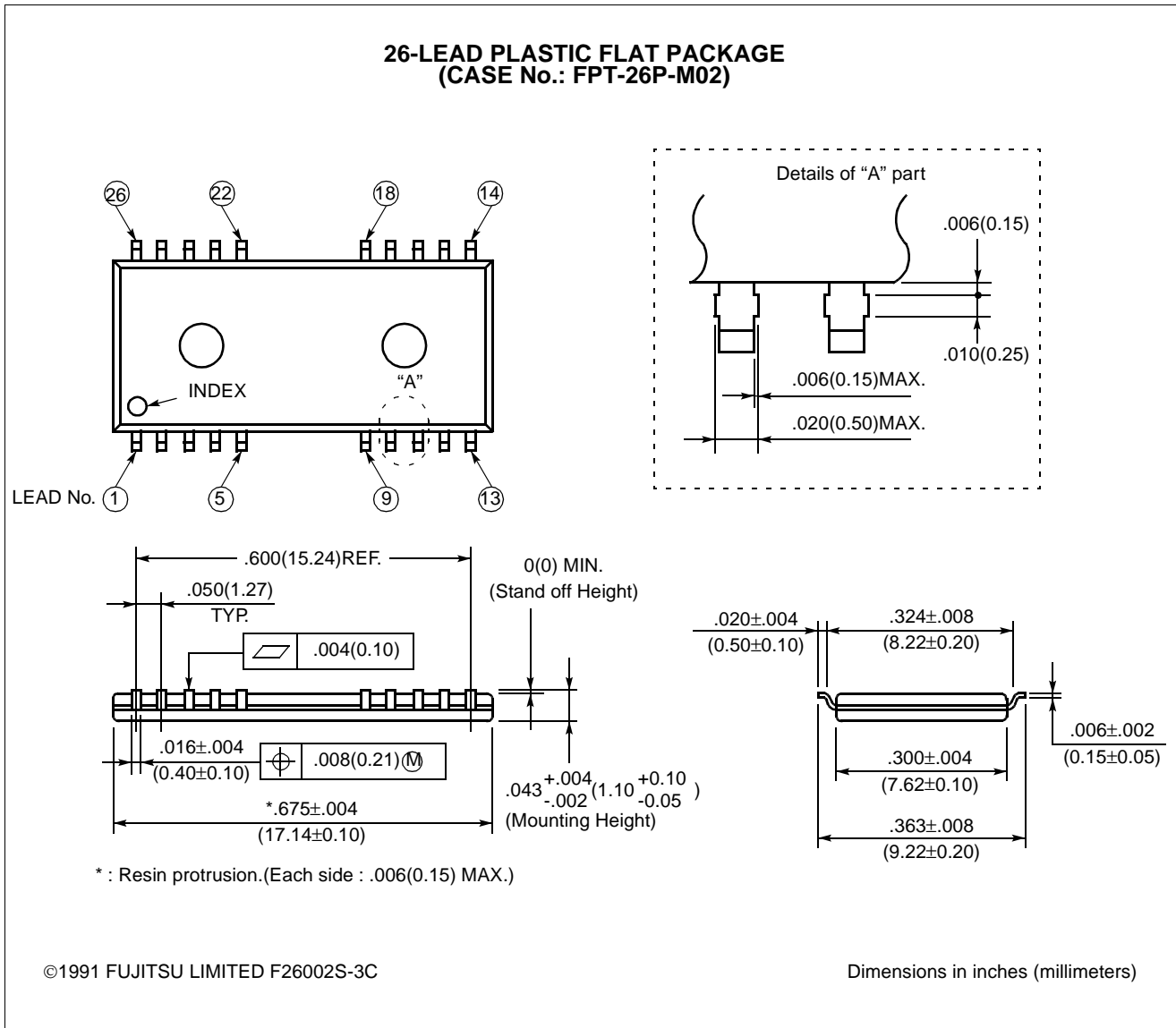
(Suffix: -PFTN)



# MB814400A-60/MB814400A-70/MB814400A-80

## ■ PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTR)



# MB814400A-60/MB814400A-70/MB814400A-80

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